OPERATION MANUAL

MODEL S500S1024

DIGITAL CORRELATION SPECTROMETER

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1. SPECIFICATION

a. Clock Input
This input is AC coupled and accepts sine or square wave with amplitude in the range of 0.5 to 1 V peak-to-peak. The frequency of the clock ranges from 1 MHz to 1 GHz. The return loss at this input is greater than 15 dB over the specified frequency range.

b. Signal Input
This input is AC coupled and accepts noise signals, received typically from the IF section of a radio-telescope, with a maximum analog bandwidth ranging from 1 MHz to 500 MHz. The power at this input should be from -3 dBm to +3 dBm for a 500 MHz bandwidth noise signal. If CW signals are used at this input, the amplitude should be in the range of 10 mV to 1V peak-to-peak. The return loss at this input is greater than 15 dB over the maximum frequency range. To avoid aliasing, always use a low-pass filter appropriate for the selected clock frequency.

c. Parallel Port
The parallel port of the S500S1024 digital correlation spectrometer should be connected to the EPP parallel port LPT2 (at address 278H) of a personal computer running the Windows 95 operate system.

d. Frequency Resolution
The S500S128 calculates and displays 1024 frequency channels of the power spectrum of band limited input signal. The frequency resolution is calculated as the signal bandwidth divided by the 1024 frequency channels. At the maximum signal bandwidth of 500 MHz the frequency resolution is 0.5 MHz. Frequency resolution can be increased by decreasing the clock frequency and thus the bandwidth.

e. Integration Time
The integration time can be set from 100 ms to 22 seconds at the maximum clock frequency of 500 MHz. The maximum integration time increases proportionally with the decrease in clock frequency because the integration counter is synchronized with submultiple signal derived from the digitizer clock.

f. Dimensions and Weight
The S500S1024 digital correlation spectrometer is enclosed in a 19 inch rack mountable box with a height of 13 inches and a depth of 24 inches. (H=330mm, W=426mm, D=610mm). Net weight is approximately 50 lb (24 Kg).

g. Power Requirements
100-240 V , 50-60 Hz, 300 VA

h. Temperature
Operating range: From 0^{O}C to 45^{O}C. Maintain a clearance of about 10 inches to ensure adequate air flows, otherwise the temperature in the enclosure will exceed the specified requirements. The instrument is protected with a temperature cut-off switch which is thermally activated at 45^{O}C and will disconnect the AC power from the instrument.
Storage range: From -40^{O}C to 75^{O}C.

i. Humidity
Maximum humidity : 95%RH at 40^{O}C.

2. THEORY OF OPERATION

Digital correlation spectrometers are used for measuring an estimate of the power spectral density of signals corrupted by noise. In most practical applications, the noise is approximated as a Gaussian random process with zero averages and the signals are assumed ergodic, independent, and small relative to the noise. When the combination of Gaussian noise with this type of signals has an extremely small signal-to-noise ratio, it is often referred to as partially coherent noise signals, or noise-like signals, or simply noise signals.

The estimate of the power spectral density of a band-limited noise signal could be generated in real-time with the S500S1024 digital correlation spectrometer which comprises a digitizer, eight digital correlator chips (S500C128A), and a parallel port interface to a personal computer system (Fig. 1). The digitizer is a special type of analog-to-digital converter which quantizes and samples the noise signal. The correlator digital chip, a special-purpose integrated circuits, calculates the correlation function of the noise signals. Finally, the general-purpose computer system performs a correction of the correlation function to remove some of the quantization errors introduced by the digitizer, calculates a fast Fourier transform of the corrected correlation function and displays an estimate of the power spectral density.

The digitizer used in the S500S1024 digital correlation spectrometer resembles a conventional analog-to-digital converters in that both perform quantization and sampling. However, they are different in the way decision levels and weights are assigned to the quantizers. Additionally, the digitizer is relatively simple since sufficiently accurate estimates of the power spectra could be obtained with the S500S1024 correlation spectrometer even when noise signals are coarsely quantized on four levels -- each sample being represented by only 2 bits.

For a band-limited noise signal quantized on four levels and sampled at the Nyquist frequency, the digital representation has a lower signal-to-noise ratio than the original analog noise signal by a factor of 0.87. This factor (sometimes expressed in percentages) by which the signal-to-noise ratio of a digitized signal decreases, relative to the analog noise signal, is also known as the efficiency of the digitizer. It is also customary that instead of characterizing digitizers in terms of their efficiency, the inverse of this is used and called sensitivity degradation factor. The sensitivity of the 2-bit digitizer with 4 quantization levels sampled at the Nyquist frequency is 1.14 when the decision levels of the quantizers are optimized and weighting factors are assigned to each quantization levels.

The transfer characteristic of the digitizer is illustrated in Fig. 2. The normalized rms voltage of the analog noise signal is plotted on the abscissa while the 2-bit encoded digital output states and the weights are shown on the ordinate. The analog noise signal is divided in four quantization levels by three threshold voltages Vl, Vo, and Vh which are chosen to be -0.9, 0, and +0.9 times the rms voltage of Gaussian noise, respectively. The most significant bit of the digital output word represents the sign and the least significant bit represents the magnitude of the digitized analog noise signal. If the voltage of the analog noise signal is positive then the sign bit is assigned the logic value 1 or 0 if it is negative. The magnitude bit is assigned the logic value 0 if the voltage of the analog noise signal is between Vl and Vh and it is assigned the logic value 1 if it is outside those two threshold voltages. Additionally, weighting factors -3, -1, +1, and +3 are assigned to the four digital output states 01, 00, 10, and 11, respectively. The choice of the value of these weights gives a uniform step of two units from one digital state to any adjacent one.

Maintaining correct threshold levels in the digitizer in terms of the rms voltage of the Gaussian noise input is much more difficult than another procedure that is based on the counts of the relative frequency of occurrence of different digital states. To implement a threshold adjustment procedure based on the frequency of occurrence it is necessary to connect to the digitizer output four frequency counters C01, C00, C10, and C11, for counting the number of samples that occur in each digital state 01, 00, 10, and 11, respectively.

Correct setting of threshold voltages is performed with Gaussian noise applied at the analog input of the digitizer. The correct threshold voltage for Vo is attained when the contents of C01+C00 and that of C10+C11 are equal, because the total number of samples with the negative sign bit equals the total number of samples with the positive sign bit. The digitizer is optimized when the threshold voltage Vh operates at 0.9 times the rms voltage of Gaussian noise input which corresponds to setting Vh such that 36.8% of the samples with the positive sign bit (C10+C11) are in counter C11. Similarly, VI should be adjusted so that 36.8% of the samples with the negative sign (C01+C00) are in counter C01. A simplified schematic diagram of the 2-bit, 4-level digitizer with the capability of setting threshold voltages based on the contents of four frequency counters located on the first S500C128 chip is depicted in Fig. 3.

The S500C128A is special-purpose custom CMOS integrated circuits, implemented as a 2x2 array of correlator cells (Fig. 4), which calculates an estimate of the correlation function between a set of digitized data inputs X and another set of digitized data inputs Y. Each set of data inputs X and Y comprises an even (E) data input and a odd (O) data input. Furthermore, each even and odd data input is encoded on two bits -- one representing a sign (S) bit and the other a magnitude (M) bit.

For reliable operation, all digitized data inputs are differential (dual-rail) with one true rail and another complementary rail labeled as bar (B). For each digitized data input, there is a corresponding data output with a label terminating in O rather than in I. The same input data appears at a corresponding output after a fixed number of clock cycles. For example, the X, even (E), magnitude (M), differential data input is labeled as (XEMI,XEMBI) and its corresponding differential data output is labeled (XEMO,XEMBO).

The S500C128 chip calculates a 128-point estimate of the correlation function between the X and Y signals sampled at a maximum data rate of 1 Gs/s and digitized in four quantization levels with weighting factors of -3, -1, +1, and +3. Consequently, the correlator chip can analyze signals with a maximum frequency of 500 MHz and has 87% of the signal-to-noise ratio of a continuous correlator. The 500 MHz bandwidth is accomplished with a clock frequency of 500 MHz (not 1 GHz) because the 2x2 array of correlator cell processes data in parallel with a time multiplexing factor of 2.

A correlator cell calculates the cross-correlation function of a prompt input signal (P_{IN}) and a delayed input signal (D_{IN}). The D_{IN} signal is generated with a tapped shift register while the P_{IN} signal is broadcast undelayed, relative to D_{IN} to all lags. Each lag computes correlation products from the P_{IN} and D_{IN} signals and subsequently accumulates these products in a counter.

The correlator cell comprises four shift registers for the digitized data. Two of the shift registers are for the P_{IN} and two more shift registers are for the D_{IN}. One of the two shift registers is for the sign bit and the other one is for the magnitude bit. A simplified block diagram of a correlator cell showing only one of the shift register for the P_{IN} and another one for the D_{IN} appears in Fig. 5. The shift register for the P_{IN} has an output tap after each flip-flop while the taps of the D_{IN} shift register are located after every two flip-flops. Each lag is made of a 2x2 bit multiplier, a 3-bit accumulator, a 32-bit counter, and four 32-bit buffer/shift registers. The contents of the accumulator can not be read out from a correlator chip. Only the contents of the four buffer/shift registers can be read out by a computer.

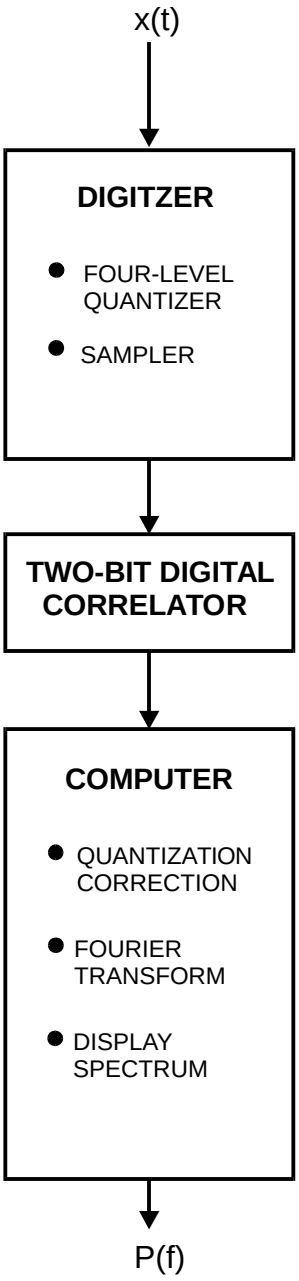
The logic diagram of one of the 2x2-bit pipelined multiplier-accumulators is shown in Fig. 6. The overflow of the multiplier-accumulator is integrated by a 32-bit counter. The 32-bit counter is implemented with conventional toggle flip-flops made from static CMOS gates. In order to allow the carry to propagate through the counter, before transferring the data to the buffer register, a synchronized gate circuit is used to isolate the counter from the accumulator. The 32-bit buffer register is designed to receive data in parallel from the counter. In one mode of operation the buffer register receives 32-bits of data from the counter and in another mode the data from the

buffer are shifted out from the chip by a host computer. The synchronized gate circuit is used to interrupt the connection between the prescaler and the counter without chopping the signal.

The procedure for reading out the contents of the counters is as follows. First, the inputs of all the counters are disconnected from the outputs of the accumulator by a control signal labeled *GCI* (Gate Counter Input). (Note that the names of the control signals that appear in italic indicate that the corresponding inputs and outputs are electrically compatible with TTL levels.) Second, the correlation coefficients accumulated in the counters are transferred to one of the 32-bit shift registers by asserting control signal *TCI* (Transfer Counter Input). Third, all the counters are set to zero by control signal *CLRI* (Clear Input). Fourth, the *GCI* control signal is activated to reconnect the inputs of the counters to the outputs of their corresponding accumulator, so that a new calculation of correlation coefficients can be made. Finally, the correlation coefficients residing now in one of the shift registers are shifted out through the *SDO* (Shift Data Out) port, one bit a time in synchronism with the *SCI* (Shift Clock Input). The *SDI* (Shift Data Input) is provided for testing the shift register, The read out starts with the highest numbered lag (lag 127) and continues in descending order of lags. Additionally, the bits of odd lags are shifted out in descending order and those of even lags in ascending order.

A correlator cell comprises 64-lags which operate at a clock frequency of 500 MHz with a bandwidth of 250 MHz. The longest integration time is determined by the 32-bit counter. At a clock frequency of 500 MHz, the correlator chip can accumulate, without overflowing, for approximated 22 seconds. The shortest integration time is determined by the interval of time required to read out the contents of the buffer/shift registers.

The idle time (blanking) of the correlator is reduced substantially by attaching a buffer registers to each. This way, only one clock cycle is required to transfer all 32 bits of the counters to the attached buffer registers. After the transfer, all the counters are cleared and the computation of correlation continues. The contents of the buffer registers are read out concurrently with a computational of new correlation coefficients. It is estimated that the blanking time (the time to transfer the contents of the counters to the buffers) of the proposed correlator will not exceed 10 nsec. The short blanking time is useful in the observation of short events such as solar flares. The contents of the buffer registers will be read out at a maximum read-clock frequency of 50 MHz.



Restriction on the input signal, x(t):

1) Must be a gaussian random signal
2) Must have a band-limited power spectrum, P(f) = 0 for f > Bw

Quantizing operation as shown in Fig. 2

Sampling frequency, Fs = 2Bw
Each sample is a two-bit digital number every Ts seconds, $Ts = \frac{1}{Fs}$

Calculates a two-bit, four level correlation function.

Correlation takes place for T seconds.

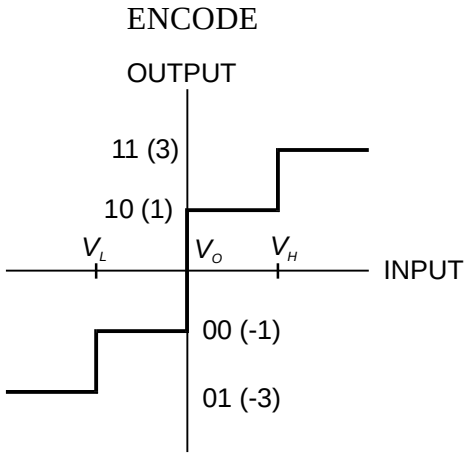
The correlation functions is read out of the correlator and is fed into a computer.

The errors caused by quantization are corrected.

The spectral estimate is computed as a Fourier transform of the correlation function.

The spectrum is displayed.

Fig. 1 Block diagram of a digital correlation spectrometer



MULTIPLY
THEN SET 1 TO 0

SdMd \ SpMp	00	01	11	10
00	0	3	-3	0
01	3	9	-9	-3
11	-3	-9	9	3
10	0	-3	3	0

DIVIDE BY 3

SdMd \ SpMp	00	01	11	10
00	0	1	-1	0
01	1	3	-3	-1
11	-1	-3	3	1
10	0	-1	1	0

ADD 3

SdMd \ SpMp	00	01	11	10
00	3	4	2	3
01	4	6	0	2
11	2	0	6	4
10	3	2	4	3

BIT 2

SdMd \ SpMp	00	01	11	10
00		1		
01	1	1		
11			1	1
10			1	

BIT 1

SdMd \ SpMp	00	01	11	10
00	1		1	1
01		1		1
11	1		1	
10	1	1		1

BIT 0

SdMd \ SpMp	00	01	11	10
00	1			1
01				
11				
10	1			1

$$\text{BIT 0} = \overline{\text{Md} + \text{Mp}}$$

$$\text{BIT 1} = \text{BIT 0} + \text{Md.Mp} \oplus (\text{Sd} \oplus \text{Sp})$$

$$\text{BIT 2} = \overline{\text{BIT 0} + \text{Sd} \oplus \text{Sp}}$$

Fig. 2 The transfer function of an optimized 2-bit 4-level digitizer

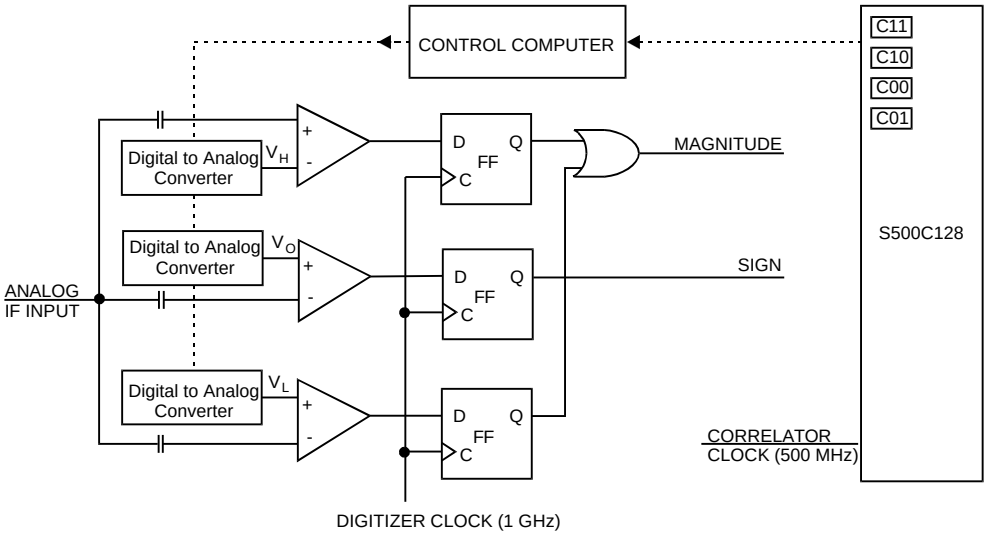


Fig. 3 A digitizer with the capability of setting threshold voltages based on the contents of four frequency counters

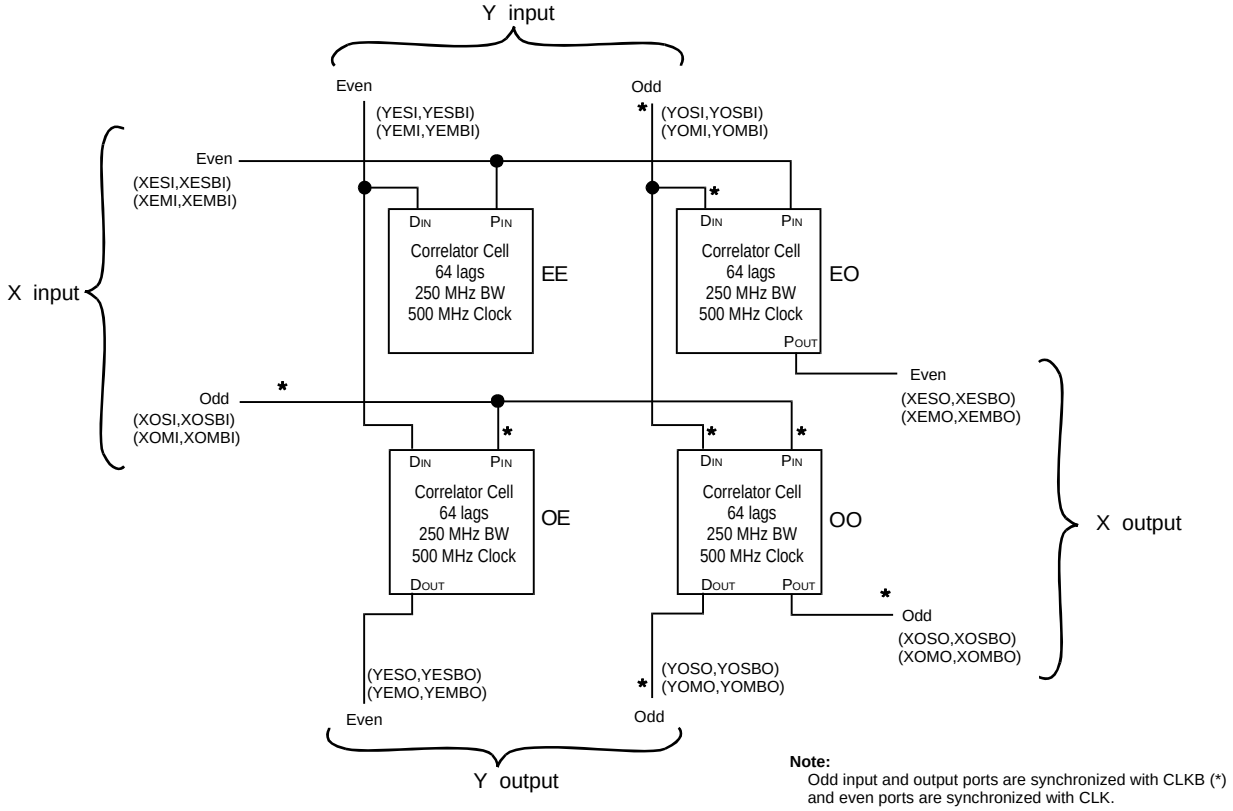


Fig. 4 The parallel processing architecture of the 128-lag correlator comprises a 2x2 array of correlator cells and uses a time multiplexing factor of 2 to achieve a bandwidth of 500 MHz at a clock frequency of 500 MHz

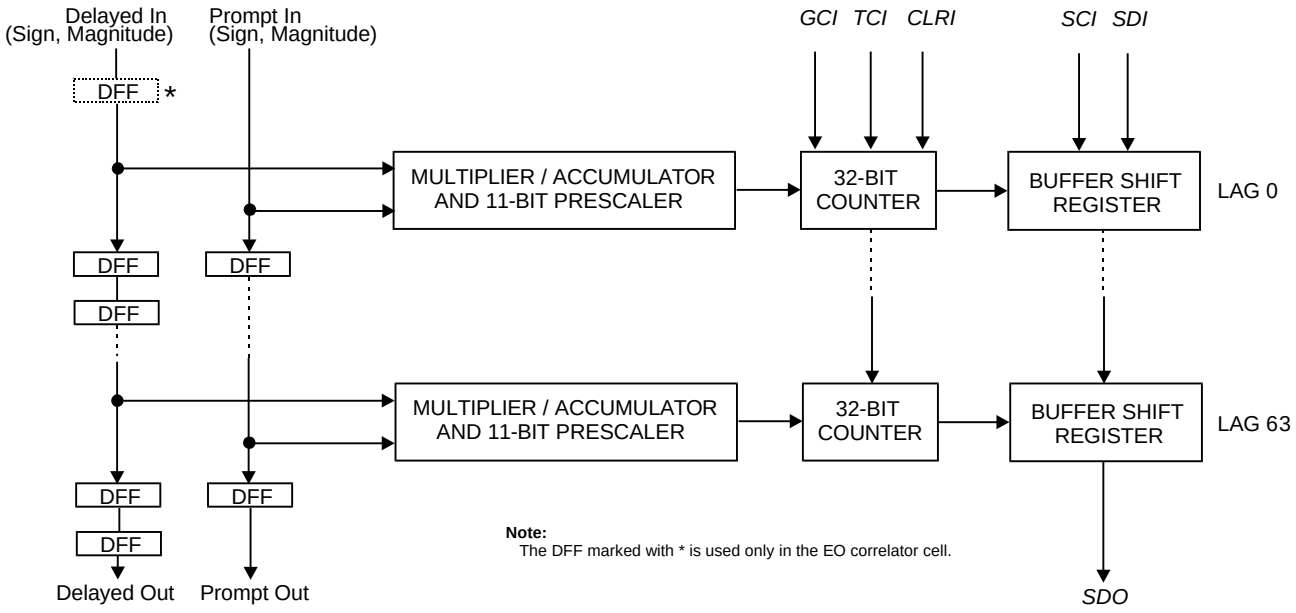


Fig. 5 A simplfied diagram of a correlator cell with 64 lags, 250 MHz bandwidth, and 500 MHz clock.

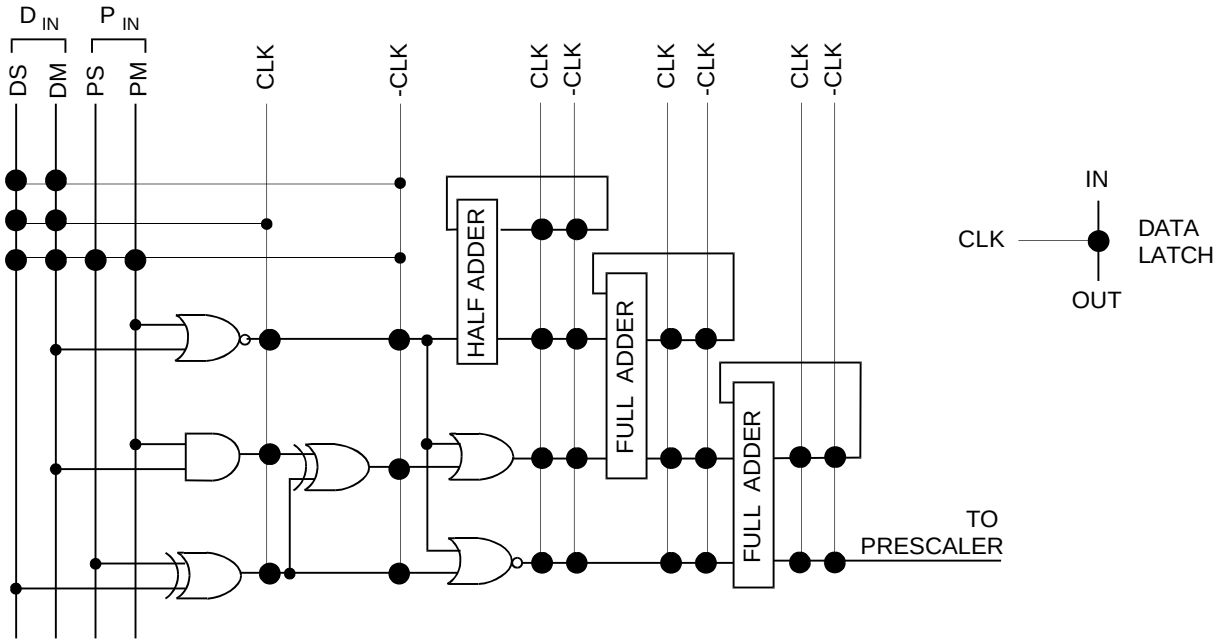


Fig. 6 The pipelined modified 2x2-bit multiplier-accumulator

3. PROGRAMMING NOTES

A. Correlation Spectrometer System

The auto-correlation spectrometer comprises a 2-bit digitizer, two programmable Xilinx chips, nine delay lines, a temperature sensor, two RF switches, and eight correlator chips (S500C120A). The 2-bit digitizer has three digital-to-analog converters for threshold voltage adjustment. The Xilinx chips contain a PC interface circuit, and an integration timer. The delay lines are Motorola MC100E195. The correlator chips are 128-channel, 2-bit, 4-level correlator.

The integration timer is implemented in the Xilinx chip on the digitizer board. The integration timer is a 32-bit count-down counter. The clock to the integration timer is derived from the system clock through a 10-bit prescaler, i.e., the clock to the integration timer equal the system clock divide by 2 to the power 10. (See section E for setting procedure.)

The three digital-to-analog converters used on the digital correlation spectrometer board are Analog Devices AD1861. They have the following features: 18-bit, 2's complement, serial input. (See section F for adjustment procedure.)

A Motorola (MC100E195) 128-step programmable delay line is used to provide the delay between the clock and the data input of the chips. This delay line has 17 ps digital step resolution. (See section G for setting procedure.)

A National Semiconductor temperature sensor (LM35DM) is placed near the on the heat sink to monitor the temperature. This sensor is used in combination with a Linear Technology A/D converter (LTC1286).

B. Enhanced Parallel Port

The digital correlation spectrometer communicates with a PC through an Enhanced Parallel Port (EPP). The EPP has the following features:

Port Name	Offset	Mode	R/W	Description
SPP Data	+0	SPP/EPP	W	Standard Parallel Port data. No autostrobing.
SPP Status	+1	SPP/EPP	R	Reads the input status lines on the interface.
SPP Control	+2	SPP/EPP	W	Sets the state of the output control lines.
EPP Address	+3	EPP	R/W	Generates an interlocked address read or write cycle.
EPP Data	+4	EPP	R/W	Generates an interlocked data read or write cycle.
Not Defined	+5,6,7	EPP	N/A	May be used for 16 and 32 bit I/O.

Pin	Signal Name	In/Out	Description
1	nWRITE	Out	Active low. Low indicates a write cycle. High for a read cycle.
2-9	A/D[0:7]	Bi	Bi-directional address/data lines.
10	nINTR	In	Peripheral interrupt. Used to generate an interrupt to the host.
11	nWAIT	In	Handshake signal. Low: OK to start a cycle. High: OK to end a cycle.
12	User defined	In	Can be used differently by each peripheral.
13	User defined	In	Can be used differently by each peripheral.
14	nDATASTB	Out	Active low. Indicates a Data Read/Write cycle is in process.
15	User defined	In	Can be used differently by each peripheral.
16	nRESET	Out	Active low. Peripheral reset.

17	nADDRSTB	Out	Active low. Indicates an Address Read/Write cycle is in process.
18-25	GND		

C. Address Space of the Correlation Spectrometer

The addresses of the correlation spectrometer are distributed as follow:

Address for WRITE		Usage
00h - 03h		write four bytes of the integration timer.
04h		load the integration timer and let it counts down.
05h		set shift data for a threshold voltage D/A.
06h		set shift clock for a threshold voltage D/A.
07h		chip select of D/A of VT0.
08h		chip select of D/A of VTL.
09h		chip select of D/A of VTH.
0Ah		control RF switch for clock source.
0Bh		control RF switch for data source.
10h		send a latch enable to the first delay line (board).
11h		send a latch enable to the second delay line (chip 1).
12h		send a latch enable to the third delay line (chip 2).
13h		send a latch enable to the fourth delay line (chip 3).
14h		send a latch enable to the fifth delay line (chip 4).
15h		send a latch enable to the sixth delay line (chip 5).
16h		send a latch enable to the seventh delay line (chip 6).
17h		send a latch enable to the eighth delay line (chip 7).
18h		send a latch enable to the ninth delay line (chip 8).
19h		send delay value into the Xilinx buffer register.
1Ah		latch five controlling bits into the Xilinx buffer register.
1Bh		set the control mode (1=auto, 0=manual).
1Ch		set the swap mode (0=no swap, 1=swap bit ordered).
1Dh	Bit 0	control CS of temperature ADC (0=select, 1=not select).
	Bit 1	clock for temperature ADC.

Address for READ	Usage
10h	read a formatted byte from the first correlator chip.
11h	read a formatted byte from the second correlator chip.
12h	read a formatted byte from the third correlator chip.
13h	read a formatted byte from the forth correlator chip.
14h	read a formatted byte from the fifth correlator chip.
15h	read a formatted byte from the sixth correlator chip.
16h	read a formatted byte from the seventh correlator chip.
17h	read a formatted byte from the eight correlator chip.
18h	read byte 0 of temperature ADC.
19h	read byte 1 of temperature ADC (only least significant 4 bits).

D. Configuring the Xilinx Chips

a. Send 0Bh to base+2 to turn on Xilinx reprogram signal.
b. Send 0Fh to base+2 to turn off Xilinx reprogram signal.
c. Wait until bit 5 at base+1 goes high.
d. Send one configuration bit to bit 0 (for Xilinx on digitizer board) and one configuration bit to bit 1 (for Xilinx on correlator board) at address base+0.
e. Send 0Dh to base+2 to turn on configuration clock.
f. Send 0Fh to base+2 to turn off configuration clock.

Repeat steps d to f until all configuration bits are sent.
Repeat steps e to f about 25 more times to wake up the Xilinx chips.

g. The Xilinx is ready when bit 4 at base+1 goes high.
h. Send 04h to base+2 to activate parallel port EPP mode.

E. Setting the Integration Timer

Write the integration timer

a. Send 00h to base+3 (EPP address port).
b. Send byte 0 to base+4 (EPP data port).
c. Send 01h to base+3 (EPP address port).
d. Send byte 1 to base+4 (EPP data port).
e. Send 02h to base+3 (EPP address port).
f. Send byte 2 to base+4 (EPP data port).
g. Send 03h to base+3 (EPP address port).
h. Send byte 3 to base+4 (EPP data port).

Set control mode to auto

i. Send 1Bh to base+3 (EPP address port).
j. Send 01h to base+4 (EPP data port).

Load and start the integration timer

k. Send 04h to base+3 (EPP address port).
l. Send 01h to base+4 (EPP data port).

F. Adjusting the Threshold Voltage

Send 18-bit control data to the D/As serially, MSB first. Each bit is sent as follow:

a. Send 05h to base+3 (EPP address port).
b. Send one bit from control data to base+4 (EPP data port).
c. Send 06h to base+3 (EPP address port).
d. Send 01h (shift clock high) to base+4 (EPP data port).
e. Send 00h (shift clock low) to base+4 (EPP data port).

Select which threshold voltage D/A

f. Send 07h (07h for VT0, 08h for VTL, 09h for VTH) to base+3 (EPP address port).
g. Send 01h to base+4 (EPP data port).
h. Send 00h to base+4 (EPP data port).

G. Adjusting the Clock Delay

On the correlator board, there are a clock delay line for the board and for each correlator chip. The delay line can be adjusted in 128 steps (7 bits), each with 17 ps. To adjust a delay line, first send the delay value to the board, then send a latch enable to the delay line to be adjusted.

a. Send 19h to base+3 (EPP address port).
b. Send delay value to base+4 (EPP data port).
c. Send a select value (10h to 18h) to base+3 (EPP address port).
d. Send 01h to base+4 (EPP data port).
e. Send 00h to base+4 (EPP data port).

H. Reading the Correlator Counters

The content of each correlator chip are shifted out serially into the Xilinx. Inside the Xilinx, every 8 bits are converted to a byte. For a fully populated board, 8 serial shifted streams are done at the same time. For each correlator chip, the read out starts with the highest numbered lag (lag 127) and continues in descending order of lags, then counter 01, counter 00, counter 10, and counter 11. Additionally, the bits of odd lags, counter 01, and counter 10 are shifted out in descending order and those of even lags, counter 00, and counter 11 in ascending order. Thus, it is necessary to swap the bit when one reads the content of the even lags, counter 00, and counter 11.

The content of the correlator can be read out at a precise interval by using the integration timer in the Xilinx on the digitizer board. The following sequence is used to read the content of the correlator.

Polling to check for the terminate signal (active low) of the integration timer:

a. Read base+1 and check bit 6.

Switch the control mode (address 1B) from 1 (auto) to 0 (manual):

b. Send 1Bh to base+3 (EPP address port).
c. Send 00h to base+4 (EPP data port).

Set the swap mode to no swap

d. Send 1Ch to base+3 (EPP address port).
e. Send 00h to base+4 (EPP data port).

Provide eight shift clocks. Do g and h eight times

f. Send 1Ah to base+3 (EPP address port).
g. Send 01h to base+4 (EPP data port).
h. Send 00h to base+4 (EPP data port).

Read one byte from each correlator chip.

i. Send 10h to base+3 (EPP address port).
j. Read the first correlator from base+4 (EPP data port).
k. Send 11h to base+3 (EPP address port).
l. Read the second correlator from base+4 (EPP data port).
m. Send 12h to base+3 (EPP address port).
n. Read the third correlator from base+4 (EPP data port).
o. Send 13h to base+3 (EPP address port).

p. Read the forth correlator from base+4 (EPP data port).
q. Send 14h to base+3 (EPP address port).
r. Read the fifth correlator from base+4 (EPP data port).
s. Send 15h to base+3 (EPP address port).
t. Read the sixth correlator from base+4 (EPP data port).
u. Send 16h to base+3 (EPP address port).
v. Read the seventh correlator from base+4 (EPP data port).
w. Send 17h to base+3 (EPP address port).
x. Read the eighth correlator from base+4 (EPP data port).

Repeat from steps f through x three more times to read all 32 bits of the counter of a lag. Next, change the swap mode to swap (1) and repeat from steps f through x four times to read the counter of the next lag. The process is continue until all the counters are read out. Note that each correlator chip have 128 lags and four test counters. Thus, the total of counter to be read out is 132.

I. Reading the Temperature

Set chip select of the A/D converter to low

a. Send 1Dh to base+3 (EPP address port).
b. Send 0 to base+4 (EPP data port).

Send 15 converting clocks. Repeat steps c and d 15 times

c. Send 2 to base+4 (EPP data port).
d. Send 0 to base+4 (EPP data port).

Read temperature

e. Send 18h to base+3 (EPP address port).
f. Read base+4 (EPP data port).
g. Send 19h to base+3 (EPP address port).
h. Read base+4 (EPP data port).

Set chip select of the A/D converter to high

i. Send 1Dh to base+3 (EPP address port).
j. Send 1 to base+4 (EPP data port).

J. Setting the RF Switches

There are two RF switches allow the selection of the Clock source and the Data source. The following steps show an example of setting the switch for Clock source.

a. Send 0Ah to base+3 (EPP address port).
b. Send 1 (for internal or 0 for external source) to base+4 (EPP data port).

The same procedure is used when setting the switch for Data source.

a. Send 0Bh to base+3 (EPP address port).
b. Send 1 (for internal or 0 for external source) to base+4 (EPP data port).

K. Setting the DIP Switches

There are four dip switches on the digitizer board. These dip switches are used to provide feed back for EPP hand shaking signal.

If the digitizer board was used alone, set

switch 2 off
switch 3 on
switch 4 on

If the digitizer board was used with the correlator board (default setting) , set

switch 2 on
switch 3 off
switch 4 off

L. Sample programs

Two programs are enclosed with the package: Setswitc.exe and Cor1024l.exe. The first one, Setswitc.exe, is used to setting the RF source. Through this simple program, we can select the internal or external clock and data. This program must be closed before opening the second one, Cor1024l.exe. Cor1024l.exe is a main program to run the correlator system.

Without running the Setswitc.exe the clock and data can be in unknown setting, it is recommend to run the Setswitc.exe before the Cor1024l.exe every time we run the correlator system.

4. APPENDIX

S500C128A SPECIFICATION

SPACEBORNE

S500C128A
Digital Correlator

FEATURES

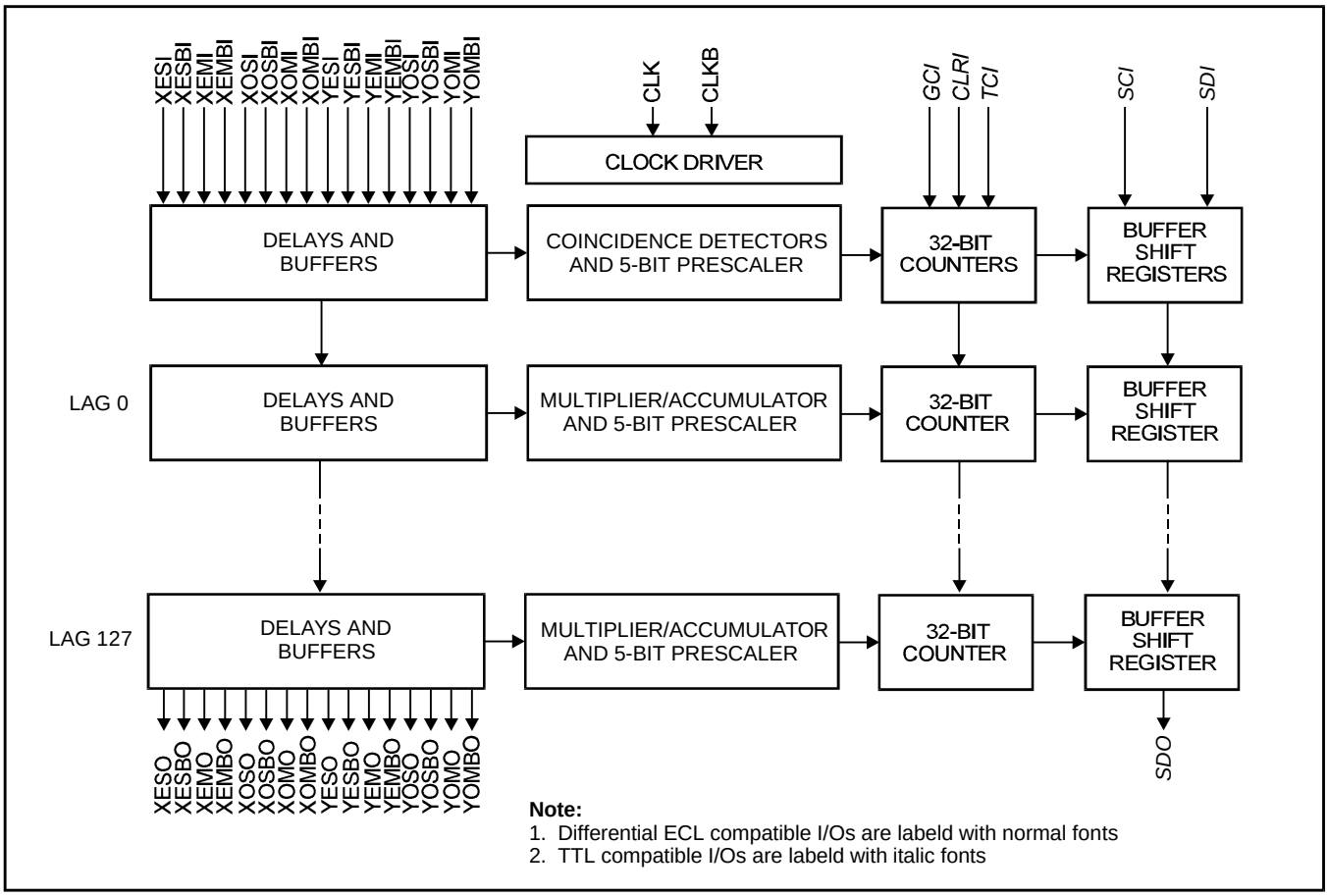
- **500 MHz Effective Signal Bandwidth**
- **500 MHz Clock Frequency**
- **2-Bit / 4 Quantization Levels**
- **128 Lags**
- **22 Seconds Max. Integration Time**
- **100 μs Min. Readout Time**
- **TTL Levels for Computer Interface**
- **Differential ECL I/O for Clock and Digitized Data**
- **Single 3.3V Power Supply**
- **12 W Power Consumption**
- **0.5 μm CMOS Fabrication Technology**

APPLICATIONS

- **Radioastronomy**
- **Atmospheric Science**
- **Frequency Allocation in Cellular Telephony**
- **Military Surveillance**

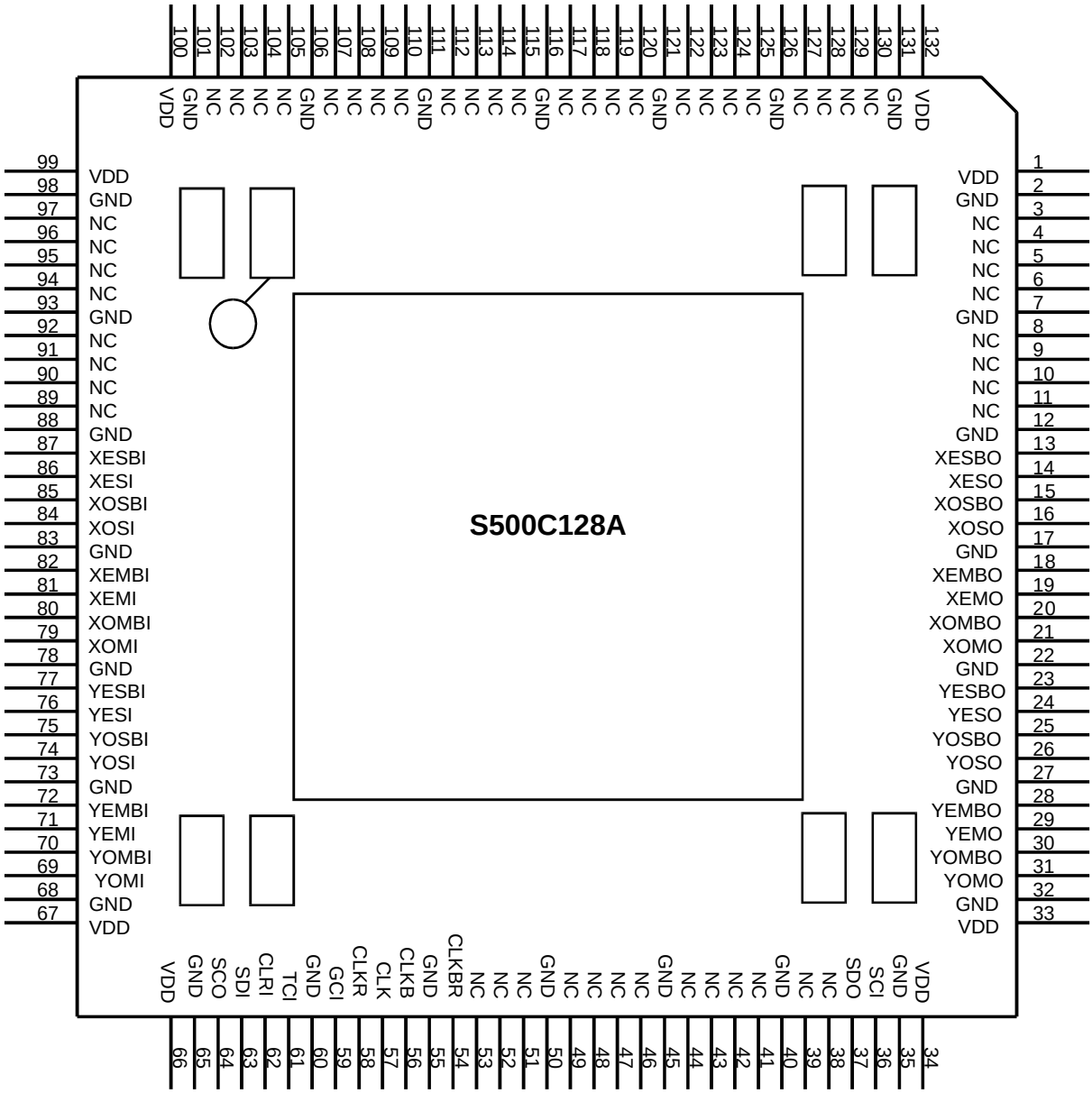
DESCRIPTION

The S500C128A is a digital correlator which calculates 128 points of the correlation function of two digitized signals. A 128-point auto-correlator with one zero lag and 127 positive (or negative) lags requires one S500C128A chip while a cross-correlator with two zero lags, 127 positive lags and 127 negative lags uses two S500C128A chips. Several S500C128A chips can be cascaded to construct correlators with more than 128 lags. The S500C128A employs a 4-level quantization scheme with weighting factors of (+3, +1, -1, -3) and a modified 2 x 2 bit multiplication table to achieve a sensitivity of 87%. The S500C128A uses parallel processing with a time multiplexing factor of 2 to achieve an effective signal bandwidth of 500 MHz at a clock frequency of only 500 MHz. Each lag comprises a 2 x 2 bit multiplier, a 5-bit prescaler, a 32-bit counter, and a 32-bit buffer shift register. The S500C128A is provided with 4 coincidence detectors and counters which contain information necessary for setting up threshold levels in a two-bit digitizer.



742 Foothill Blvd., Suite 2B, La Canada, CA 91011 Phone: (818) 952-0126 Fax: (818) 952-2635 Email: ctimoc@aol.com

PIN CONNECTIONS



GENERAL INFORMATION

The S500C128A is a special-purpose custom CMOS integrated circuit, implemented as a 2x2 array of correlator cells (Fig. 1), which calculates an estimate of the correlation function between a set of digitized data inputs X and another set of digitized data inputs Y. Each set of data inputs X and Y comprises an even (E) data input and a odd (O) data input. Furthermore, each even and odd data input is encoded on two bits -- one representing a sign (S) bit and the other a magnitude (M) bit.

For reliable operation, all digitized data inputs are differential (dual-rail) with one true rail and another complementary rail labeled as bar (B). For each digitized data input, there is a corresponding data output with a label terminating in O rather than in I. The same input data appears at a corresponding output after a fixed number of clock cycles. For example, the X, even (E), magnitude (M), differential data input is labeled as (XEMI,XEMBI) and its corresponding differential data output is labeled (XEMO,XEMBO).

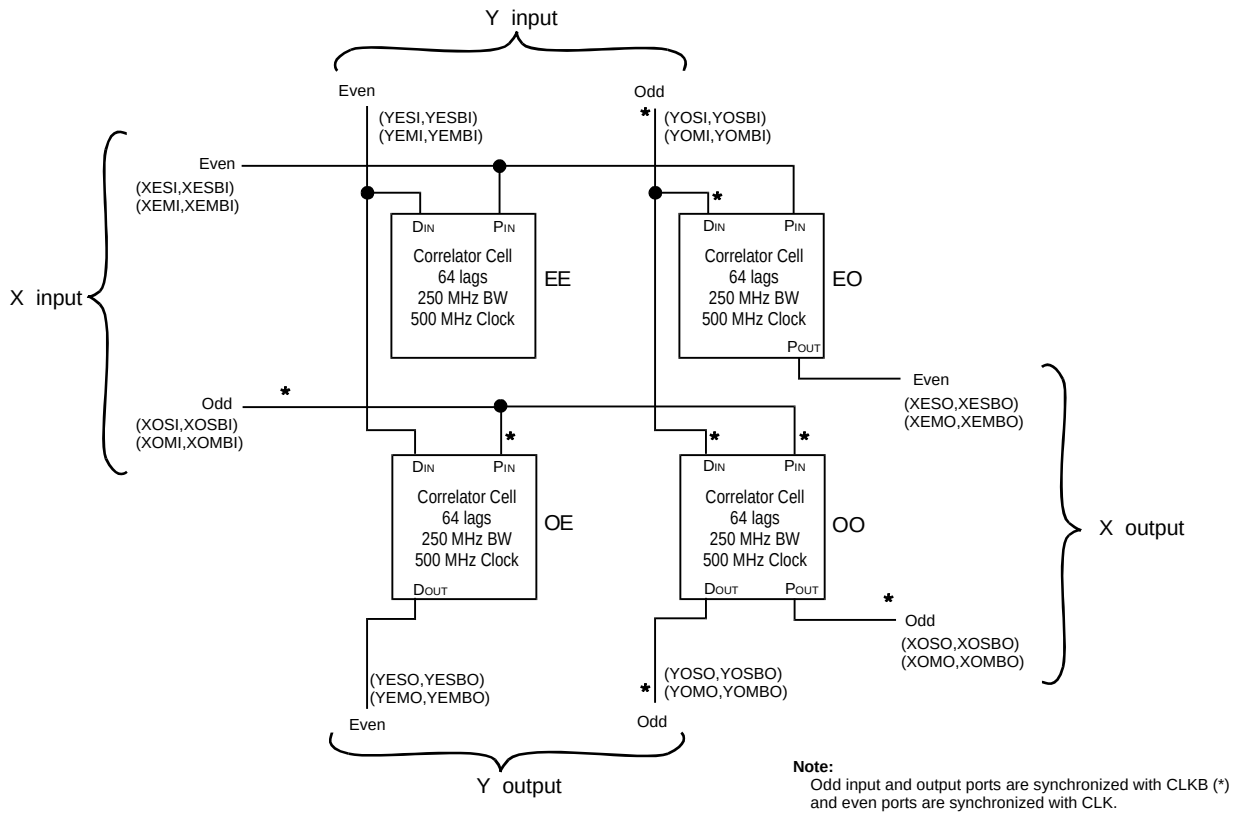


Fig. 1 The parallel processing architecture of the S500C128A is comprises of a 2x2 array of correlator cells and uses a time multiplexing factor of 2 to achieve a bandwidth of 500 MHz at a clock frequency of 500 MHz

The S500C128A calculates a 128-point estimate of the correlation function between the X and Y signals sampled at a maximum data rate of 1 Gs/s and digitized in four quantization levels with weighting factors of +3, +1, -1, and -3. Consequently, the S500C128A can analyze signals with a maximum frequency of 500 MHz and has 87% of the signal-to-noise ratio of a continuous correlator. The 500 MHz bandwidth is accomplished with a clock frequency of 500 MHz (not 1 GHz) because the 2x2 array of correlator cell processes data in parallel with a time multiplexing factor of 2.

Correlator Cell

A correlator cell comprises four shift registers for the digitized data. Two of the shift registers are for the prompt data and two more shift registers are for the delayed data. One of the two shift registers is for the sign bit and the other one is for the magnitude bit. A simplified block diagram of a correlator cell showing only one of the shift register for the prompt input and another one for the delayed input appears in Fig. 2. The shift register for the prompt input has an output tap after each flip-flop while the taps of the delayed data shift register are located after every two flip-flops.

Each lag in a correlator cell is made of a 2x2 bit multiplier, a 3-bit accumulator, and a 32-bit counter. Counters of lags with the same delay in correlator cells EE and OO are added and those in correlator cells EO and OE are added. Adding requires an extra 2-bit accumulator. Thus, from the chip point of view, each lag has a 5-bit accumulator and a 32-bit counter. Each lag also comprises a 32-bit buffer/shift register which is used for off-line reading the content of the 32-bit counter.

The procedure for reading out the contents of the counters is as follows. First, the inputs of all the counters are disconnected from the outputs of the prescalers by a control signal labeled *GCI (Gate Counter Input).* (Note that the names of the control signals that appear in italics indicate that the corresponding inputs and outputs are electrically compatible with TTL levels.) Second, the correlation coefficients accumulated in the counters are transferred to the buffer/shift registers by asserting control signal *TCI (Transfer Counter* Input). Third, all the counters are set to zero by control signal *CLRI (Clear Input).* Fourth, the *GCI* control signal is activated to reconnect the inputs of the counters to the outputs of their corresponding prescalers, so that a new calculation of correlation coefficients can be made. Finally, the correlation coefficients residing now in the buffer/shift register are shifted out through the *SDO (Shift Data Out)* port, one bit a time in synchronism with the *SCI (Shift Clock Input).* The *SDI (Shift Data Input)* is provided for testing the buffer/shift register. The read out starts with the highest numbered lag of the S500C128A (lag 127) and continues in descending order of lags. Additionally, the bits of odd lags are shifted out in descending order and those of even lags in ascending order.

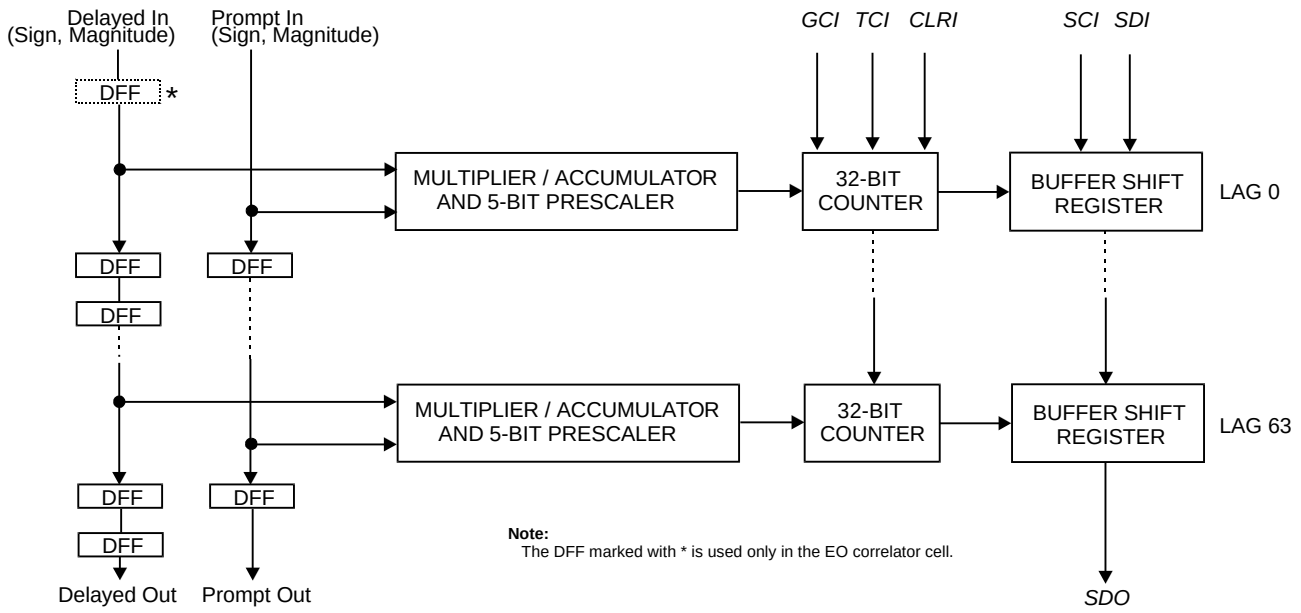
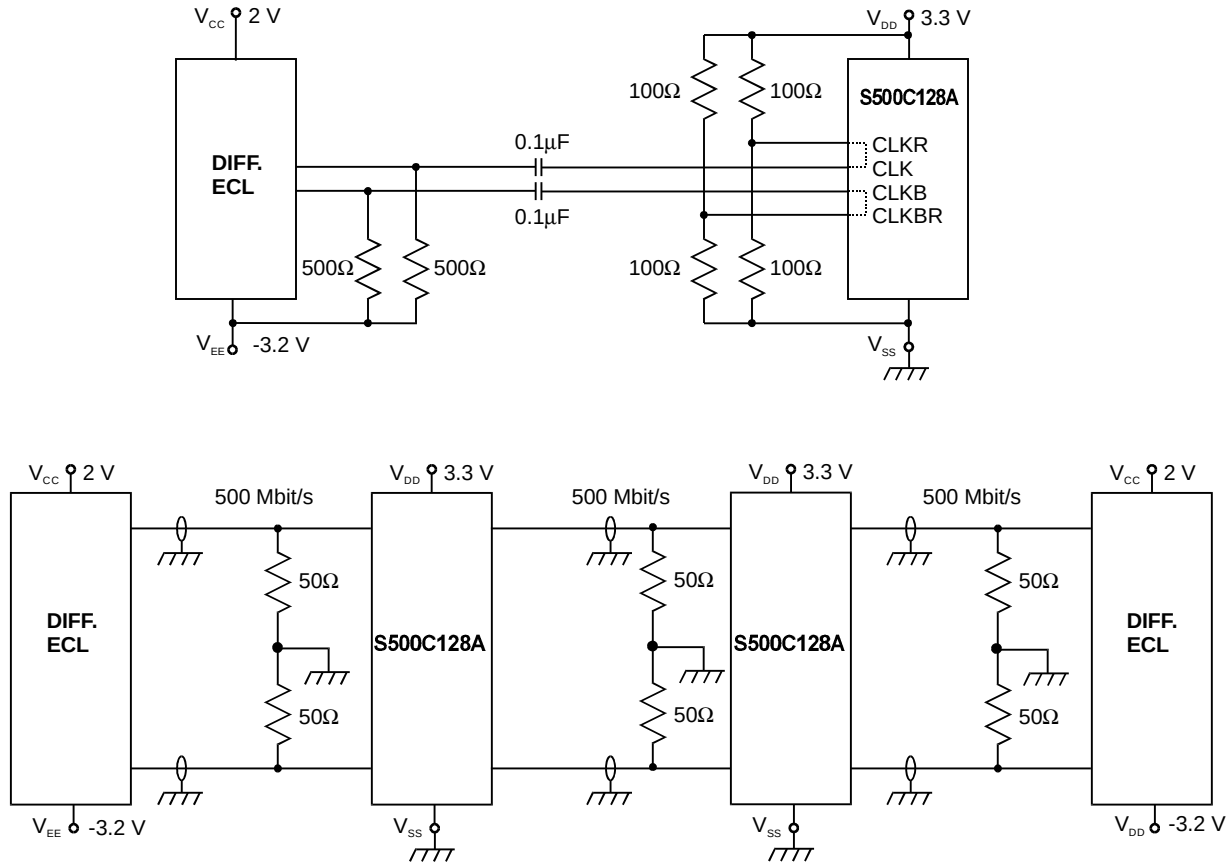


Fig. 2 A simplfied diagram of a correlator cell with 64 lags, 250 MHz bandwidth, and 500 MHz clock.

A correlator cell comprises 64-lags which operate at a clock frequency of 500 MHz with a bandwidth of 250 MHz. The longest integration time is determined by the 5-bit equivalent accumulator and the 32-bit counter. At a clock frequency of 500 MHz, the S500C128A can accumulate, without overflowing, for 22 seconds. The shortest integration time is determined by the interval of time required to read out the contents of the buffer/shift registers. A complete read out can be performed in 100 μs with a *SCI (Shift Clock Input)* of 50 MHz.

Digitized Data and Clock Interfacing

To facilitate the construction of large correlator systems with thousands of lags, several S500C128A correlator chips can be connected in a cascade configuration -- the outputs X and Y of one correlator chip can be DC connected via transmission lines to the inputs X and Y, respectively, of another correlator chip (Fig. 3). The pin assignments of the S500C128A package is such that the X and Y outputs of one correlator package can be connected to the X and Y inputs, respectively, of another correlator package via transmission lines parallel with each other. Since the output pins of one package are aligned with the coressponding inputs of another package, the transmission lines between two packages can be made as short as 7 mm (0.3 in.). The communication between S500C128A chips is accomplished over 50 ohm transmission lines at a maximum data rate of 500 Mbit/s.



Note: Two transmission lines, each with a characteristic impedance of 50Ω, form one differential transmission line.

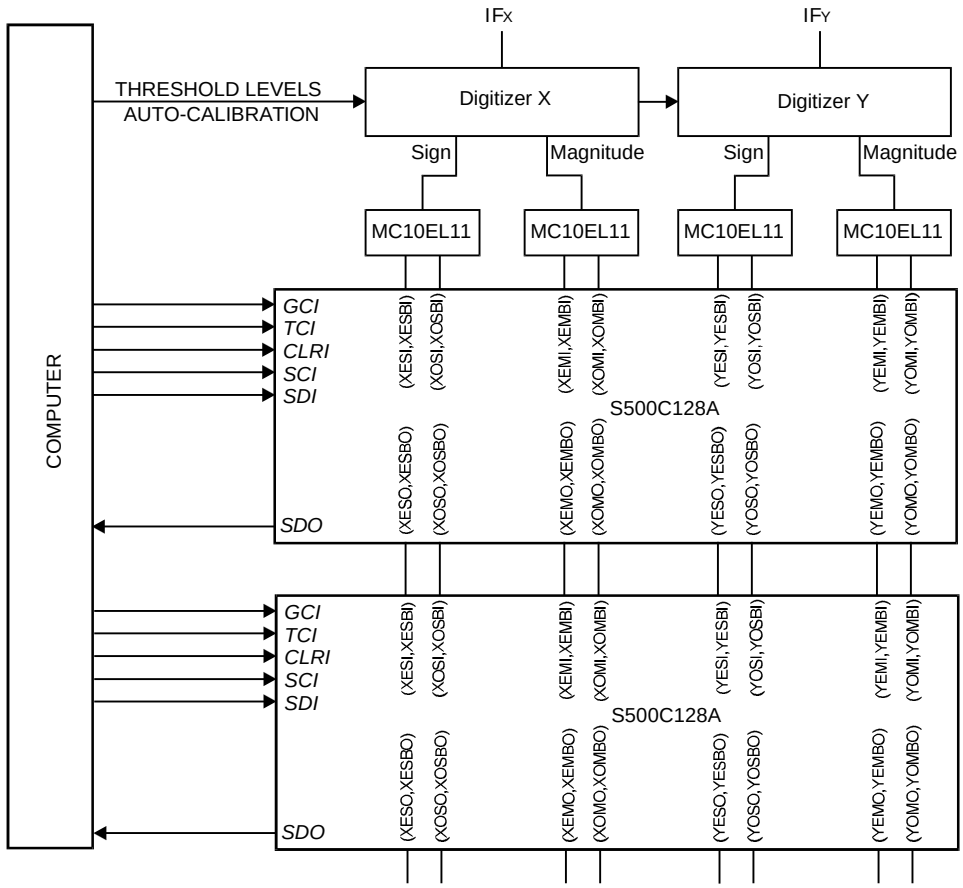
Fig. 3 Interfacing the S500C128A with other similar chips and with differential ECL integrated circuits.

The S500C128A can communicate directly with differential ECL integrated circuits. Since the S500C128A operates between a positive power supply of 3.3 V and ground, the power supply of the ECL chips has to be shifted such that their Vtt is at the ground potential. The communication between S500C128A chips and differential ECL chips via 50 ohm transmission lines is performed at a maximum data rate of 500 Mbit/s.

Cross-Correlating Spectrometer

A digital cross-correlating spectrometer (Fig. 4) is used to generate the cross-power spectrum of two analog input signals. It comprises two digitizers, two S500C128A chips connected positive lags as cross-correlators, and a general purpose computer. Each digitizer performs quantization and sampling of an IF (Intermediary Frequency) analog signal. The digitized data is encoded on two bits -- a sign bit and a magnitude bit. Both the sign and the magnitude bits are connected to two inputs of a first S500C128A correlator chip through an ECL fan-out buffer.

Data integrated in the correlators is read out by the computer which performs a Fourier transform of the cross-correlation coefficients in order to produce a graphical representation of the cross-power spectrum. Moreover, an automatic calibration procedure is programmed in the computer to adjust threshold voltages of the digitizers based on information from a set of four coincidence counters residing in the correlators.



Note: MC10EL11 are ECL fan-out buffers made by Motorola

Fig. 4 A 256-lag, 500 MHz bandwidth cross-correlating spectrometer using two cascaded S500C128A correlator chips.

The digitizers are operated at a clock frequency of 1 GHz in order to sample correctly IF signals with a maximum frequency of 500 MHz. Due to the parallel processing scheme used in the S500C128A correlators, they are capable of processing digitized data with a maximum rate of 1 Gs/s at a clock frequency of 500 MHz. Although only a positive 256-lag system is shown, spectrometer systems with thousands of positive and negative lags can be realized by cascading several S500C128A correlator chips.

Digitizer

The S500C128A is designed to operate with a digitizer in which the IF input signal is quantized with weighting factors (3, 1, -1, and -3), assigned to the four possible levels of the quantizer (Fig. 5). The operation of the four-level quantizer is presented in the form of a transfer characteristic in which the abscissa is the normalized voltage of the IF signal and the ordinate is the corresponding two-bit encoded digital output.

The input IF signal is distributed to three comparators with threshold voltage levels set at Vh, Vo, and Vl, respectively. Each threshold voltage is generated by a digital-to-analog converter controlled with a computer from information collected in four coincidence counters (C11, C10, C00, C01) located in the S500C128A. Counters C10 and C00 record the number of samples above and bellow Vo, respectively, and counters C11 and C01 record the number of samples above Vh and bellow Vl, respectively.

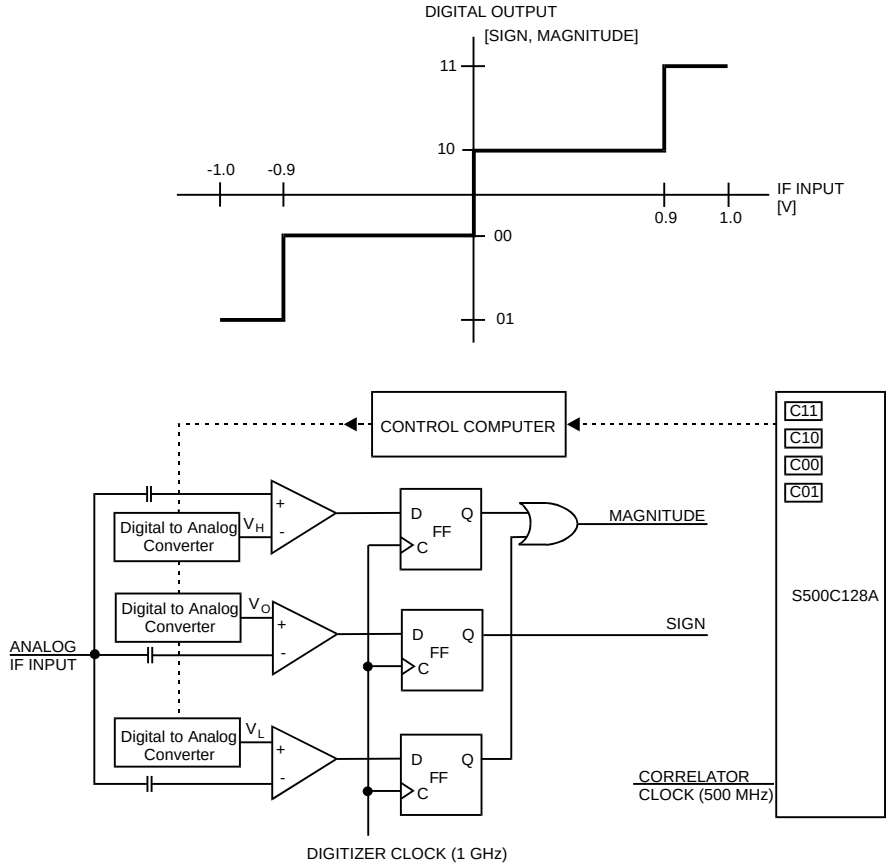


Fig. 5 A four-level, 500 MHz bandwidth digitizer with self-calibration capability and the transfer function of its quantizer

Threshold voltage settings are performed with Gaussian noise. The correct threshold voltage setting for Vo is achieved when the content of C11+C10 and that of C00+C01 are equal. Threshold voltages Vh and Vl are set such that the content of C11 is equal to 36.8% of the content of C11 + C10 and the content of C01 is 36.8% of C00 + C01, respectively. In terms of the rms voltage of the IF signal, these settings correspond to Vo= 0 Vrms, Vh=0.9 Vrms, and Vl=-0.9 Vrms.

The output of each comparator is sampled by a flip-flop clocked at a maximum frequency of 1 GHz to achieve a maximum bandwidth of 500 MHz. The S500C128A correlator chip achieves the same bandwidth with a clock frequency of 500 MHz.

PIN DESCRIPTION

Name	QFP Pin	Type	Description
VDD	1, 33, 34, 66, 67, 99,100, 132	Power	Positive power supply can be from 2 V to 3.3 V
GND	2, 7, 12, 17, 22, 27, 32, 35, 40, 45, 50, 55, 60, 65, 68, 73, 78, 83, 88, 93, 98, 101, 106, 111, 116, 121, 126, 131	Ground	
GCI	59	TTL input	The ***G***ate ***C***ounter ***I***nput is an asynchronous signal that disconnects the prescalers from the counters. When *GCI* is high, all the counters stop counting. When *GCI* goes low, all the counters start counting.
TCI	61	TTL input	The ***T***ransfer ***C***ounter ***I***nput tranfers the content of the counters to the buffer/shift registers. Transferring happens when *SCI* (***S***hift ***C***lock ***I***nput) is at a logic low and a positive pulse is applied to the *TCI* input for a minimum duration of 10 ns.
SCI	36	TTL input	The ***S***hift ***C***lock ***I***nput is used to shift out the content of the buffer/shift registers. When the *TCI* input is at a logic low, the content of the buffer shift registers are shifted out on the falling edge of *SCI*. This signal can have a maximum frequency of 50 MHz.
CLRI	62	TTL input	The ***CL***ea***R*** ***I***nput is asynchronous. When the *CLRI* goes high and stays high for a minimum 20 ns, the contents of the counters are reset to zeroes.
SDI	63	TTL input	The ***S***hift ***D***ata ***I***n signal is the data input of the buffer/ shift register. It can be used for testing the buffer/shift register.
SDO	37	TTL output	The ***S***hift ***D***ata ***O***ut is used to obtain the contents of the buffer/shift register serially. The content of the buffer/shift register of lag 127 is shifted out fist with the most significant bit first. The content of the buffer/shift register of lag 126 is shifted out next with the least significant bit first. The shifting is finished with the most significant bit of the buffer/shift register of the first coincidence detector.

Name	QFP Pin	Type	Description
CLK, CLKB	56, 57	Diff ECL input	clock input
CLKR, CLKBR	58, 54	Diff ECL output	clock input return
XESI, XESBI	86, 87	Diff ECL input	X even sign
XEMI, XEMBI	81,82	Diff ECL input	X even magnitude
XOSI, XOSBI	76, 77	Diff ECL input	X odd sign
XOMI, XOMBI	71, 72	Diff ECL input	X odd magnitude
YESI, YESBI	84, 85	Diff ECL input	Y even sign
YEMI, YEMBI	79, 80	Diff ECL input	Y even magnitude
YOSI, YOSBI	74, 75	Diff ECL input	Y odd sign
YOMI, YOMBI	69, 70	Diff ECL input	Y odd magnitude
XESO, XESBO	14, 13	Diff ECL output	X even sign
XEMO, XEMBO	19, 18	Diff ECL output	X even magnitude
XOSO, XOSBO	24, 23	Diff ECL output	X odd sign
XOMO, XOMBO	29, 28	Diff ECL output	X odd magnitude
YESO, YESBO	16, 15	Diff ECL output	Y even sign
YEMO, YEMBO	21, 20	Diff ECL output	Y even magnitude
YOSO, YOSBO	26, 25	Diff ECL output	Y odd sign
YOMO, YOMBO	31, 30	Diff ECL output	Y odd magnitude

ABSOLUTE MAXIMUM RATINGS
(Above which the useful life may be impaired)

Storage Temperature ..... -65^{O}C to +150^{O}C
Ambient Temperature with Power Applied ..... -55^{O}C to 85^{O}C
Supply Voltage to Ground Potential ..... -0.5V to +5V
DC Input Voltage ..... -0.5V to +5V

OPERATING RANGE

VDD ..... 2 V to 3.3V
Ambient Temperature .....-55^{O}C to 85^{O}C

DC CHARACTERISTICS: VDD = 3.3V

Symbol	Parameter	25^{O}C			85^{O}C			Unit
		min	typ	max	min	typ	max	
I_{DD}	Power supply current		3.8	4		3.6	3.8	A
V_{IHTTL}	TTL high-level input voltage	2			2			V
V_{ILTTL}	TTL low-level input voltage			0.8			0.8	V
I_{OHTTL}	TTL high-level output current			-0.5			-0.5	µA
I_{OLTTL}	TTL low-level output current			20			20	mA
V_{IHECL}	ECL high-level input voltage	80			80			mV
V_{ILECL}	ECL low-level input voltage			0			0	mV
V_{OHECL}	ECL high-level output voltage	150			150			mV
V_{OLECL}	ECL low-level output voltage			0			0	mV

AC CHARACTERISTICS: VDD = 3.3V

Symbol	Parameter	25^{O}C			85^{O}C			Unit
		min	typ	max	min	typ	max	
f_{CLK}	Sine wave clock frequency		600	700		500	600	MHz
pCLK	Differential clock phase imbalance			40			40	degrees
t_{SKEW}	Skew time between any digitized inputs			100			100	ps